Amendment To The Claims

1. (Currently Amended) A graphics processor, comprising:

a receiving unit ~~first interface~~ for receiving ~~an externally input~~ a graphics command from an external unit of the processor;

a transferring unit ~~second interface~~ for performing a data transfer operation ~~between the graphic processor and a work~~ to a memory;

~~a data bus for transferring data between the first interface and the second interface;~~

a display data generation section ~~for receiving a graphics command from the data bus, generating display data by decoding the graphics command, and outputting the generated display data to the data bus~~;

an image display section for receiving the display data from the ~~data bus and displaying~~ memory to display an image on a display device; ~~and~~

~~a bus control section for monitoring a status of use of the data bus and controlling a right to use the data bus,~~

~~wherein the bus control section sets a priority for each data transfer operation along the data bus and control the right to use the data bus according to the set priorities~~

wherein the graphic command is transferred from the external unit to the memory when the external unit has a right to use the bus, and

wherein the display data generation section receives the graphics command from the memory, generates a display data by decoding the graphics command, and outputs the generated display data to the memory .

2. (Currently Amended) The graphic processor of claim 1, wherein the bus control section sets a priority for each of at least the following data transfer operations: a data transfer operation of transferring ~~an externally input~~ the graphics command to the ~~work~~ memory; a data transfer operation of supplying ~~a~~ the graphics command from the ~~work~~ memory to the display data generation section; and a data transfer operation of supplying display data from the ~~work~~ memory to the image display section.

3. (Currently Amended) The graphic processor of claim 1, further comprising a bus control section for monitoring a status of use of the data bus and controlling a right to use the data bus,

wherein the bus control section sets a priority for each data transfer operation along the data bus and controls the right to use the data bus according to the set priorities and

wherein the bus control section is configured so that a setting of the priorities of data transfer operations can be changed dynamically.

4. (Currently Amended) The graphic processor of claim 3, further comprising:

a pre-decoding section for pre-decoding a graphics command transferred during a data transfer operation of transferring ~~an externally input~~ the graphics command from a CPU to the ~~work~~ memory; and

a processing amount estimating section for estimating a data processing amount at the display data generation section based on a result of the pre-decoding by the pre-decoding section,

wherein the bus control section changes the priorities of the data transfer operation according to the data processing amount estimated by the processing amount estimating section.

5. (Currently Amended) The graphic processor of claim 4, wherein when the estimated data processing amount per a predetermined period of time exceeds a predetermined amount, the bus control section sets the priority of a data transfer operation of supplying a graphics command from the ~~work~~ memory to the display data generation section to be higher than the priority of a data transfer operation of transferring ~~an externally-input~~ the graphics command to the ~~work~~ memory.

6. (Currently Amended) The graphic processor of claim 3, further comprising a memory monitor for monitoring an amount of data of graphics commands stored in the ~~work~~ memory,

wherein the bus control section changes the priorities of the data transfer operations according to the data amount monitored by the memory monitor.

7. (Currently Amended) The graphic processor of claim 6, wherein when the monitored data amount is smaller than a predetermined amount, the us control section sets the priority of a data transfer operation of transferring an externally-input graphics command to the ~~work~~ memory to be higher than the priority of a data transfer operation of supplying a graphics command form the ~~work~~ memory to the display data generation section.

8. (Currently Amended) The graphic processor of claim 3, wherein:

the ~~first interface~~ receiving unit is connected to an external bus which is provided external to the graphic processor;

an external bus monitor for monitoring an amount of data being transferred along the external bus is connected to the external bus; and

the bus control section changes the priorities of the data transfer operations along the data bus according to the amount of data being transferred which is monitored by the external bus monitor.

9. (Original) The graphic processor of claim 1, wherein:

the display data generation section includes a graphics command storing section for temporarily storing a graphics command which is input through the data bus, and a decoding section for decoding a graphics command which is output from the graphics command storing section;

the graphics command storing section includes first data storing means and second data storing means, writes graphics commands into selected one of the first and second data storing means in a predetermined address order, and reads out graphics commands from selected one of the first and second data storing means in a predetermined address order; and

when a reading address in one of the first and second data storing means from which graphics commands are being read out matches a predetermined check address, the graphics command storing section starts writing new graphics commands into the one of the first and second data storing means.

Claims 10-11 (Cancel)

12. (New) A graphic processing system of transferring data through a bus comprising:

a central processing unit;

a memory for storing data through the bus;

a display data generation section for generating display data;

an image display section for receiving the display data from the memory to display,

wherein a graphic command is transferred from the central processing unit to the memory when the central processing unit has a right to use the bus, and

wherein the display data generation section generates the display data by decoding the graphic command received from the memory and outputs the display data to the memory.

13. (New) The graphic processing system of claim 12, wherein the central processing unit, a display data generation section, and a image display section share the bus.

14. (New) The graphic processing system of claim 12 or 13, wherein a bus control section sets a priority for each of at least the following data transfer operation:

(a) a data transfer operation for transferring the graphic command from the central processing unit to the memory through the bus,

(b) a data transfer operation for transferring the graphic command from the memory to the display data generation through the bus, and

(c) a data transfer operation for transferring the display data from the memory to the image display section through the bus.

15. (New) The graphic processing system of claim 14, wherein the data transfer operation for transferring the display data from the memory to the image display section must be given the highest priority at a time interval.

16. (New) The graphic processing system of claim 14, wherein the graphic command includes a variable-length data.

17. (New) The graphic processing system of claim 14, wherein the bus control section is configured so that a setting of the priority of data transfer operation can be changed dynamically.

18. (New) The graphic processing system of claim 17, further comprising

a pre-decoding section for pre-decoding a graphics command transferred during a data transfer operation of transferring a graphics command from the central processing unit to the memory; and

a processing amount estimating section for estimating a data processing amount at the display data generation section based on a result of the pre-decoding by the pre-decoding section;

wherein the bus control section changes the priorities of the data transfer operations according to the data processing amount estimated by the processing amount estimating section.

19. (New) The graphic processing system of claim 18, wherein when the estimated data processing amount per a certain period of time exceeds a certain amount, the bus control section sets the priority of a data transfer operation of supplying a graphics command from the memory to the display data generation section to be higher than the priority of a data transfer operation of transferring a graphics command from the central processing unit to the memory.

20. (New) The graphic processing system of claim 17, further comprising:

a memory monitor for monitoring an amount of data of graphics commands stored in the memory,

wherein the bus control section changes the priorities of the data transfer operations according to the data amount monitored by the memory monitor.

21. (New) The graphic processing system of claim 20,

wherein when the monitored data amount is smaller than a certain amount, the bus control section sets the priority of a data transfer operation of transferring an graphics command to the memory to be higher than the priority of a data transfer operation of supplying a graphics command from the memory to the display data generation section.

22. (New) The graphic processing system of claim 17, further comprising

a receiving unit which is connected to an external bus which is provided external to the graphic processor;

an external bus monitor for monitoring an amount of data being transferred along the external bus is connected to the external bus; and

the bus control section changes the priorities of the data transfer operations along the data bus according to the amount of data being transferred which is monitored by the external bus monitor.

23. (New) The graphic processing system of claim 12, further comprising

a graphics command storing section in the display data generation section storing a graphics command which is transferred from the memory temporarily,

wherein the graphics command read out according to a data use sequence, and

wherein the graphics command storing section has a check address which serves as a trigger for supplying new graphics commands to the graphics command storing section from the memory.

24. (New) The graphic processing system of claim 23,

wherein the graphics command storing section has a plurality of data storing means, stores the graphics command into selected one of the plurality of the storing means and reads out graphics commands from the selected one of the plurality of the storing means, and

wherein when a reading address in one of the plurality of the storing means from which graphics commands are being read out matches the check address, the graphics command storing section starts writing new graphics commands into the one of the plurality of the storing means.

25. (New) A system of transferring data through a bus comprising;

a central processing unit;

a memory for storing data through the bus;

a data generation section for generating data to be outputted; and

an output section for outputting a data from the memory;

wherein the command is transferred from the central processing unit to the memory when the central processing unit is given a right to use the bus by the bus control section, and

wherein a data generation section generates a data to be outputted by decoding the command received from the memory and outputs the data to the memory.

26. (New) The system of claim 25, wherein the central processing unit, the data generation section, and the output section share the bus.

27. (New) The system of claim 25 or 26,

wherein the bus control section sets a priority for each of at least the following data transfer operation:

(a) a data transfer operation for transferring a command from the central processing unit to the memory through the bus,

(b) a data transfer operation for transferring a command from the memory to the processor through the bus,

(c) a data transfer operation for transferring the data from the memory to the output section through the bus.

28. (New) The system of claim 27, wherein at least one of the data transfer must be given the highest priority at a time interval.

29. (New) The system of claim 27, wherein the graphic command includes a variable-length data.

30. (New) The system of claim 27, wherein the bus control section is configured so that a setting of the priorities of data transfer operations can be changed dynamically.

31. The system of claim 30, wherein the priority of the bus control section can be changed based on an amount of the command to be transferred from the central processing unit to the memory.